



SIGNETICS CORPORATION

INTEGRATED CIRCUITS

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August 15, 1967

SIGNETICS DCL CONTINUES TO EXPAND

DCL (Designers Choice Logic) continues to add elements to make your choice as a designer even easier. In June, we mailed you the S8000J (DCL) brochure which consists of the 8400 and 8800 series. We are now adding further elements, but before we go further, let's define:

- S8000J - Full Military Temperature Range DCL in Flat Pak
- S8000A - Full Military Temperature Range DCL in DIP
- N8000J - 0 to 70°C DCL in Flat Pak
- N8000A - 0 to 70°C DCL in DIP

Enclosed are the S8000A, N8000J and N8000A data sheets to supplement the basic DCL brochure. We have also added the following new types to assist you in minimizing can count and optimizing system efficiency:

- S8415J (S8415A, N8415J, N8415A): Dual 5 Input Low Power NAND Gate, Bare Collectors
- S8470J (S8470A, N8470J, N8470A): Triple 3 Input Low Power NAND Gate
- S8471J (S8471A, N8471J, N8471A): Triple 3 Input Low Power NAND Gate, Bare Collectors
- S8481J (S8481A, N8481J, N8481A): Quad 2 Input Low Power NAND Gate, Bare Collectors

Also enclosed are the latest data sheets on the SE518G, SE518K, NE518G and NE518K Voltage Comparator.

Please discard the following families of data sheets: NE400A, ST400A, SP400A, NE800A, ST800A and SP800A. These are replaced by the N8000A. Also the NE800J which is replaced by the N8000J.


Jack Halter
Sales Manager

JH/kda

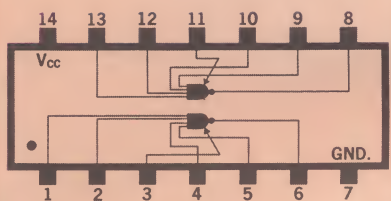


S8000A-SERIES

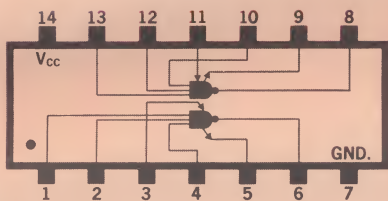
JULY 1967

The S8000A-Series of integrated circuits is functionally identical to like numbered elements in the Signetics S8000J-Series. The operating temperature range is -55°C to $+125^{\circ}\text{C}$ and the design rules and data in the S8000J data handbook apply to the S8000A-Series. Differences between the two sets of elements are related only to packaging.

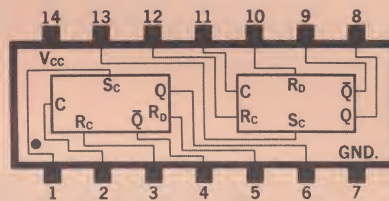
LOW POWER ELEMENTS



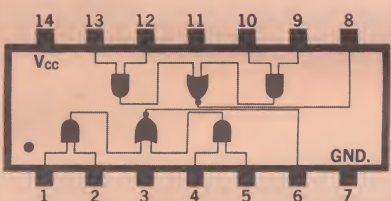
S8416A DUAL FOUR-INPUT
EXPANDABLE DTL NAND GATE



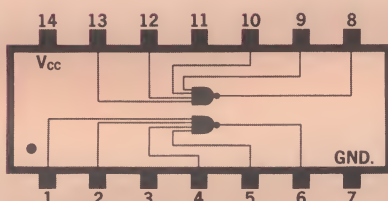
S8417A DUAL THREE-INPUT
EXPANDABLE DTL NAND GATE



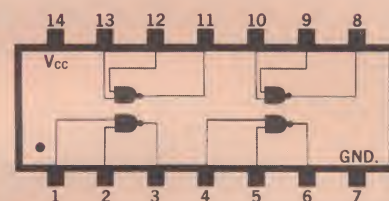
S8424A DUAL AC DTL BINARY ELEMENT



S8440A DUAL AND-OR-INVERT TTL GATE

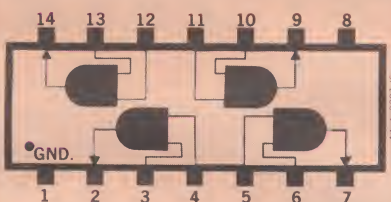


S8455A DUAL FOUR-INPUT
TTL NAND GATE DRIVER

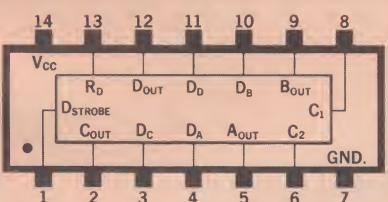


S8480A QUAD TWO-INPUT TTL NAND GATE

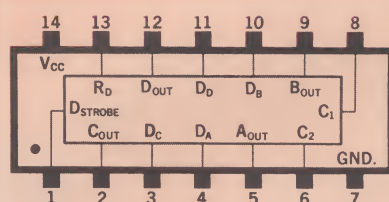
HIGH SPEED ARRAYS



S8731A QUAD TWO-INPUT DIODE EXPANDER



S8280A DECADE COUNTER



S8281A BINARY COUNTER





R _D	Asynchronous Reset
S _D	Asynchronous Set
R _C	Synchronous (Clocked) Reset*
S _C	Synchronous (Clocked) Set*
D	Data Input (Single ended)
J	Synchronous Set*
K	Synchronous Reset*



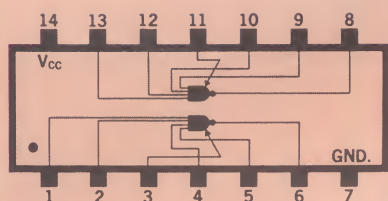
Printed in U. S. A.



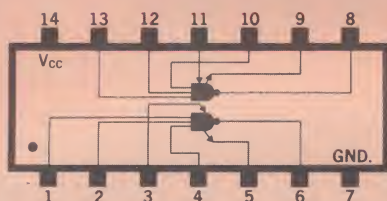
N8000A-SERIES

The N8000A-Series of integrated circuits is functionally identical to like numbered elements in the Signetics S8000J-Series. Differences between the two sets of elements are related only to temperature-dependent parameters and packaging. The operating temperature range of the N8000A-Series is 0°C to $+75^{\circ}\text{C}$ where that of the S8000J-Series is -55°C to $+125^{\circ}\text{C}$. In all other respects the design rules and data in the S8000J data handbook apply to the N8000A-Series.

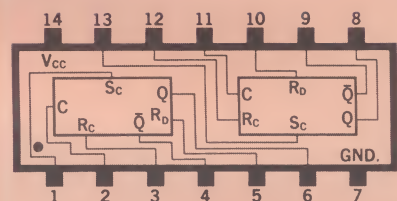
LOW POWER ELEMENTS



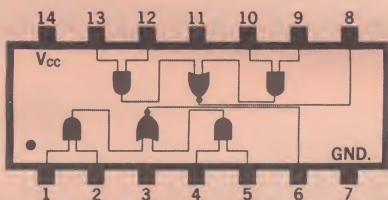
N8416A DUAL FOUR-INPUT
EXPANDABLE DTL NAND GATE



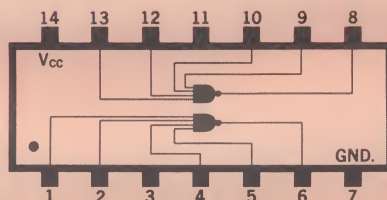
N8417A DUAL THREE-INPUT
EXPANDABLE DTL NAND GATE



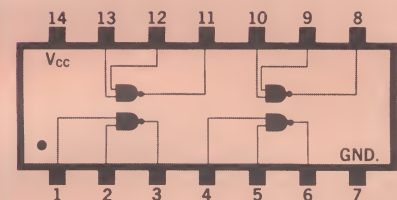
N8424A DUAL AC DTL BINARY ELEMENT



N8440A DUAL AND-OR-INVERT TTL GATE

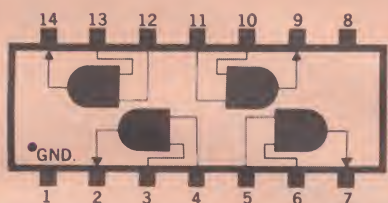


N8455A DUAL FOUR-INPUT
TTL NAND GATE DRIVER

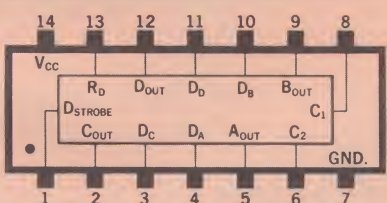


N8480A QUAD TWO-INPUT TTL NAND GATE

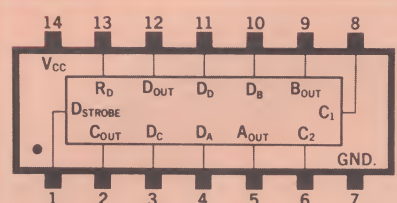
HIGH SPEED ARRAYS



N8731A QUAD TWO-INPUT DIODE EXPANDER



N8280A DECADE COUNTER



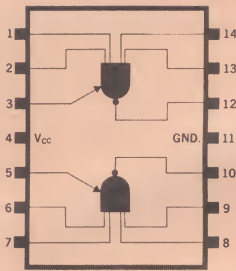
N8281A BINARY COUNTER



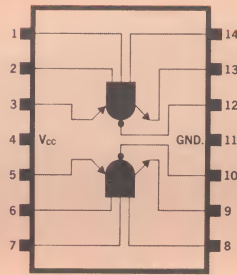
N8000J-SERIES

The N8000J-Series of integrated circuits is functionally and mechanically identical to like numbered elements in the Signetics S8000J-Series. Differences between the two sets of elements are related only to temperature-dependent parameters. The operating temperature range of the N8000J-Series is 0°C to +75°C where that of the S8000J-Series is -55°C to +125°C. In all other respects the design rules and data in the S8000J data handbook apply to the N8000J-Series.

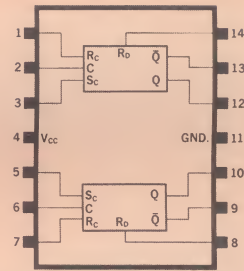
LOW POWER ELEMENTS



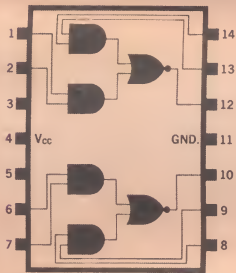
**N8416J DUAL FOUR-INPUT
EXPANDABLE DTL NAND GATE**



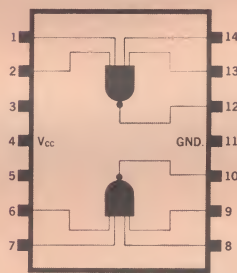
**N8417J DUAL THREE-INPUT
EXPANDABLE DTL NAND GATE**



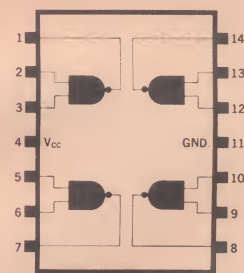
N8424J DUAL AC DTL BINARY ELEMENT



N8440J DUAL AND-OR-INVERT TTL GATE

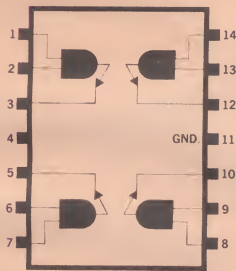


**N8455J DUAL FOUR-INPUT
TTL NAND GATE DRIVER**

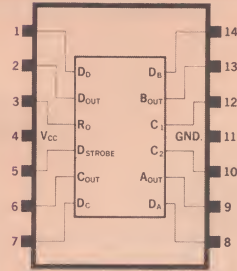


N8480J QUAD TWO-INPUT TTL NAND GATE

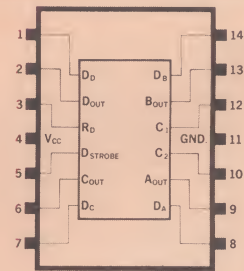
HIGH SPEED ARRAYS



N8731J QUAD TWO-INPUT DIODE EXPANDER



N8280J DECADE COUNTER



N8281J BINARY COUNTER





PRELIMINARY SPECIFICATIONS

**LOW POWER
MONOLITHIC DCL ELEMENT**



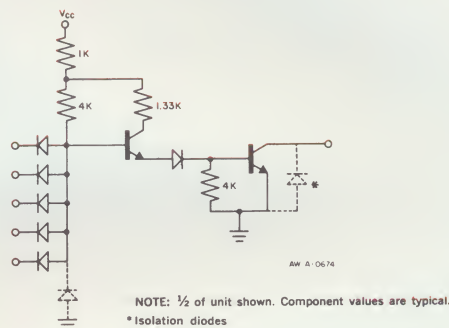
S8415A
S8415J
N8415A
N8415J

S8415A,	S8415J	DUAL	FIVE-INPUT	DTL	NAND	GATE	(-55°C to +125°C)
N8415A,	N8415J	DUAL	FIVE-INPUT	DTL	NAND	GATE	(0°C to + 75°C)

The 8415 is a Dual, 5-Input NAND Gate with bare output collectors. Absence of any output pull-up structure allows the user complete freedom in the use of the 8415 in collector-logic (wired-AND) and similar applications. Proper pull-up resistor selection will allow as many as 30 outputs to be tied together. Attention must be given to the "1" DC noise margin and the "0" fan-out when selecting a pull-up resistor.

These devices are additional elements to the S8000J product line. For electrical characteristics curves, refer to the S8417J electrical characteristic curves in the S8000J data handbook.

BASIC CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

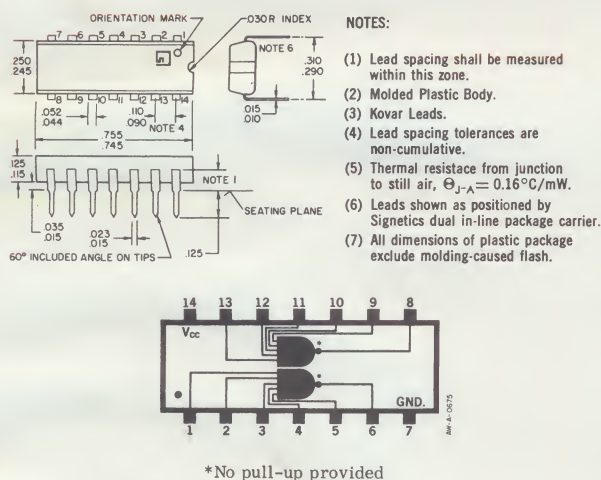
INPUT VOLTAGE	+6.0V
OUTPUT VOLTAGE	+6.0V
V _{cc}	+6.0V
INPUT CURRENT	±10mA

OUTPUT CURRENT	± 30 mA
OPERATING TEMPERATURE (S8415)	-55°C to +125°C
(N8415)	0°C to +75°C
STORAGE TEMPERATURE	-65°C to +150°C
JUNCTION TEMPERATURE	+150°C

Maximum ratings are limiting values above which serviceability may be impaired.

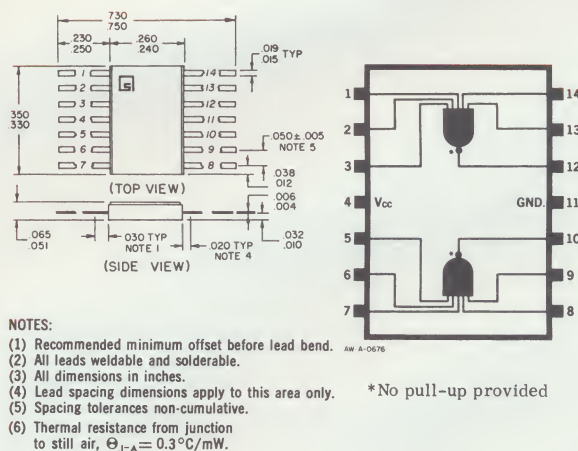
**S8415A
N8415A**

SIGNETICS A-PACKAGE



**S8415J
N8415J**

J-PACKAGE (TO-88)
(MODULAR GLASS-KOVAR)



ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 12,)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8415	TEMP. N8415	V _{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-4	"1" OUTPUT LEAKAGE CURRENT			40	μA	+125°C	+75°C	5.0V	0.7V			11
A-5	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	8.2mA	8
A-3				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	8.2mA	8
A-4				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	8.2mA	8
C-1	"0" INPUT CURRENT	-0.1		-1.2	mA	-55°C	0°C	5.25V	0.35V	5.25V		
A-3		-0.1		-1.2	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-1.2	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	0V			
A-6	PAIR DELAY (Figure 1)	50		150	ns	+25°C	+25°C	5.0V			D.C. F.O. = 9	9
C-2	FALL TIME (Figure 2)			75	ns	-55°C	0°C	4.75V			A.C. F.O. = 2	10
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			20	mW	+25°C	+25°C	5.0V				
	(Per Gate) OUTPUT "1"			6.5	mW	+25°C	+25°C	5.0V	0V			
A-2	INPUT VOLTAGE RATING	6.0			V	+25°C	+25°C	5.0V	50μA	0V		
A-2	OUTPUT VOLTAGE RATING	6.0			V	+25°C	+25°C	5.0V	0V			13

NOTES

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. $f = 1\text{MHz}$, $V_{ac} = 25\text{mVrms}$. All pins not specifically referenced are tied to guard for capacitance tests.
8. Output sink current is supplied through a resistor to V_{cc} .
9. One DC fan-out is defined as 0.8mA.
10. One AC fan-out for the 8400 Gates is defined as the clock input of an 8424 or 50pf.
11. Connect an external 1K ± 1 percent resistor from V_{cc} to the output terminal for this test.
12. Manufacturer reserves the right to make design and process changes and improvements.
13. Connect an external 1K ± 1 percent resistor from 6.3V to the output terminal.

FIGURE 1 — PAIR DELAY

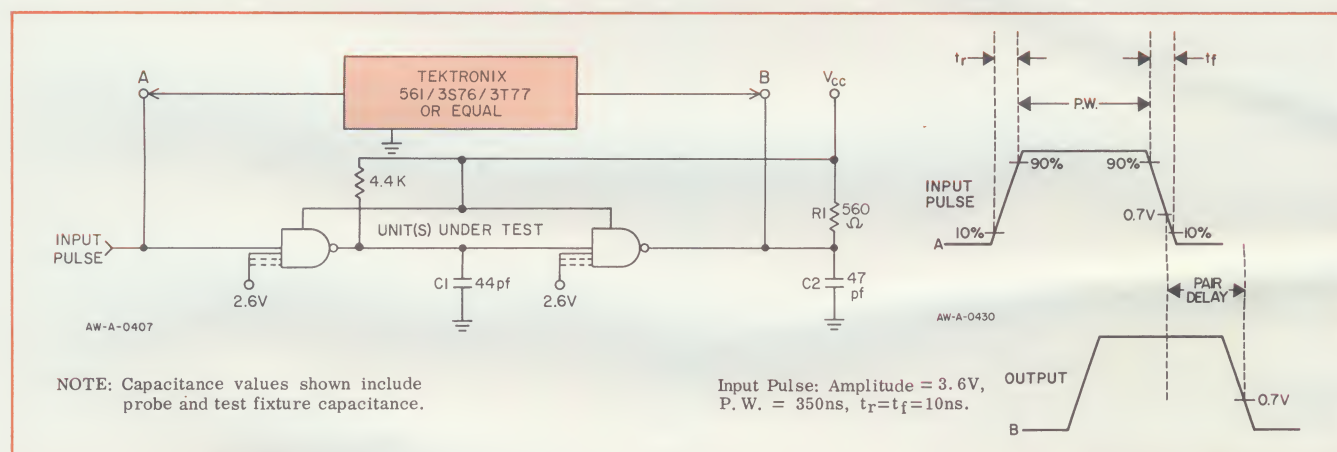
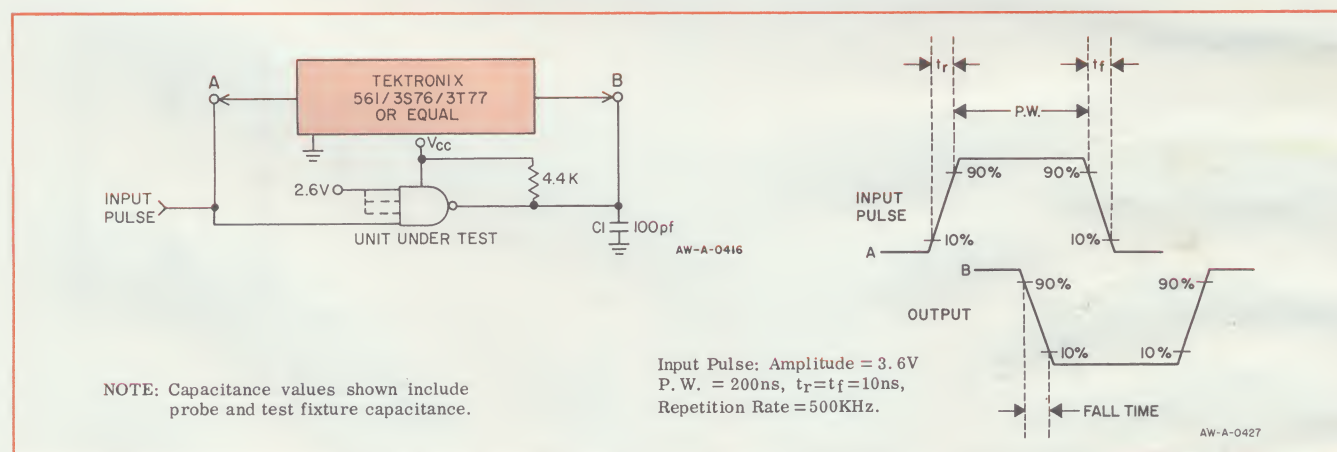


FIGURE 2 — FALL TIME



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ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 12,)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8470	TEMP. N8470	V _{CC}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5 A-3 A-4	"1" OUTPUT VOLTAGE	3.4 3.6 3.4			V	-55°C +25°C +125°C	0°C +25°C +75°C	4.75V 5.0V 4.75V	0.7V 0.7V 0.7V		-225μA -225μA -225μA	8 8 8
A-5 A-3 A-4	"0" OUTPUT VOLTAGE			0.35 0.35 0.35	V	-55°C +25°C +125°C	0°C +25°C +75°C	4.75V 5.0V 4.75V	2.0V 2.0V 2.0V	2.0V 2.0V 2.0V	7.2mA 7.2mA 7.2mA	9 9 9
A-5 A-3 C-1	"0" INPUT CURRENT	-0.1 -0.1 -0.1		-0.8 -0.8 -0.8	mA	-55°C +25°C +125°C	0°C +25°C +75°C	5.25V 5.25V 5.25V	0.35V 0.35V 0.35V	5.25V 5.25V 5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	PAIR DELAY (Figure 1)	25		95	ns	+25°C	+25°C	5.0V			D.C. F.O.=9	10
C-2	OUTPUT FALL TIME (Figure 2)			75	ns	-55°C	0°C	4.75V			A.C. F.O.=2	11
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0" (Per Gate) OUTPUT "1"			15.0 4.5	mW mW	+25°C +25°C	+25°C +25°C	5.0V 5.0V	0V 0V			
A-2	INPUT VOLTAGE RATING	6.0			V	+25°C	+25°C	5.0V	50μA	0V		
A-2	OUTPUT SHORT CIRCUIT CURRENT	-4.0		-12.0	mA	+25°C	+25°C	5.0V	0V		0V	

NOTES

- All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- All measurements are taken with ground pin tied to zero volts.
- Positive current flow is defined as into the terminal referenced.
- Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
- Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
- Measurements apply to each gate element independently.
- Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. $f = 1\text{MHz}$, $V_{AC} = 25\text{mV}_{\text{rms}}$. All pins not specifically referenced are tied to guard for capacitance tests.
- Output source current is supplied through a resistor to ground.
- Output sink current is supplied through a resistor to V_{CC} .
- One DC fan-out is defined as 0.8mA.
- One AC fan-out for the 8400 Gates is defined as the clock input of an 8424 or 50pf.
- Manufacturer reserves the right to make design and process changes and improvements.

FIGURE 1 — PAIR DELAY

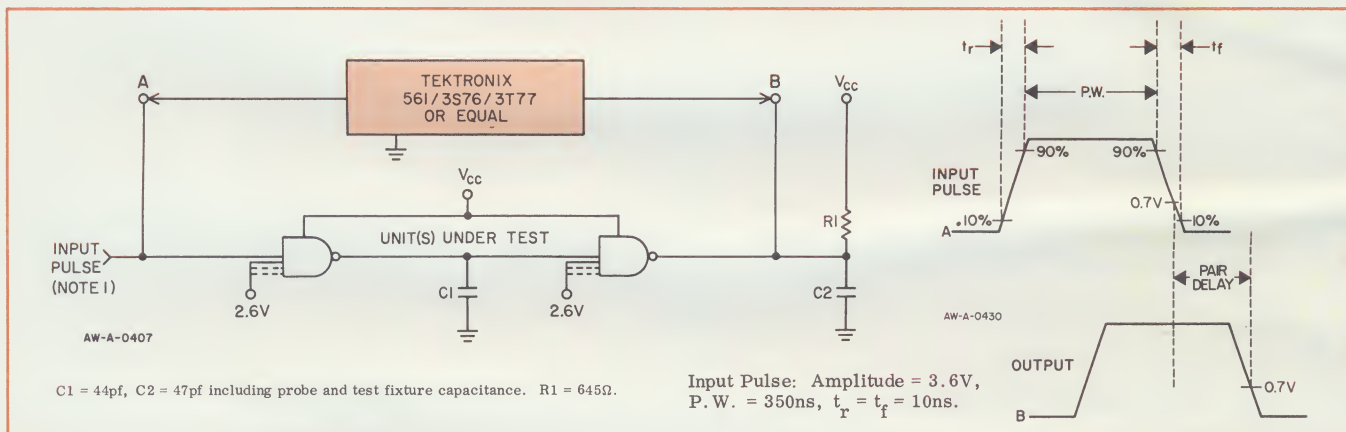
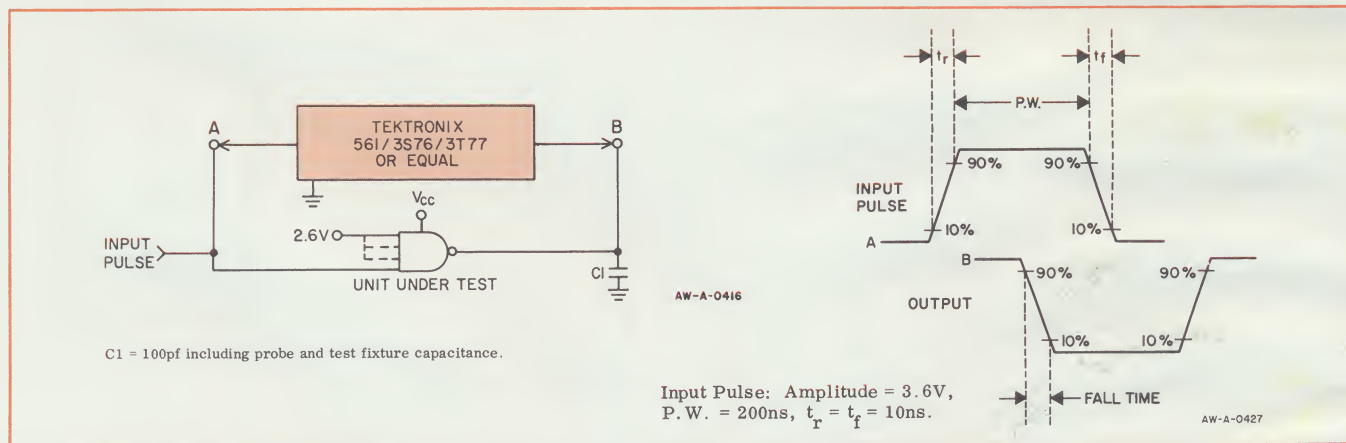


FIGURE 2 — FALL TIME

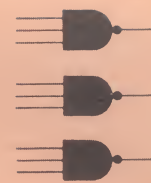


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PRELIMINARY SPECIFICATION

LOW POWER MONOLITHIC DCL ELEMENT



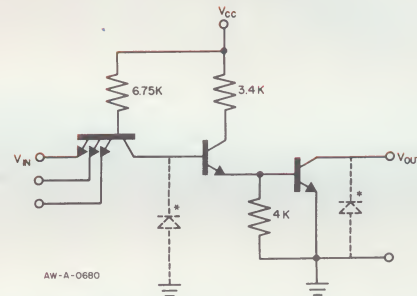
S8471A
S8471J
N8471A
N8471J

S8471A, S8471J TRIPLE THREE-INPUT TTL NAND GATE (−55°C to +125°C)
N8471A, N8471J TRIPLE THREE-INPUT TTL NAND GATE (0°C to + 75°C)

The 8471 is a Triple, 3-Input NAND Gate with bare output collectors. Absence of any output pull-up structure allows the user complete freedom in the use of the 8471 in collector-logic (wired-AND) and similar applications. Proper pull-up resistor selection will allow as many as 30 outputs to be tied together. Attention must be given to the "1" DC noise margin and the "0" fan-out when selecting a pull-up resistor.

These devices are additional elements to the S8000J product line. For electrical characteristic curves, refer to the S8480J electrical characteristic curves in the S8000J data handbook.

BASIC CIRCUIT SCHEMATIC



NOTE: 1/2 of unit shown. Component values are typical.
* Isolation diodes

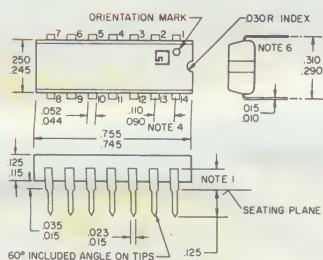
ABSOLUTE MAXIMUM RATINGS

INPUT VOLTAGE	+6.0V
OUTPUT VOLTAGE	+6.0V
V _{CC}	+6.0V
INPUT CURRENT	±10mA

Maximum ratings are limiting values above which serviceability may be impaired.

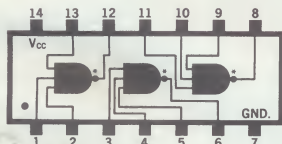
OUTPUT CURRENT	+30, −10mA
OPERATING TEMPERATURE (S8471) (N8471)	−55°C to +125°C 0°C to +75°C
STORAGE TEMPERATURE	−65°C to +150°C
JUNCTION TEMPERATURE	+150°C

S8471A N8471A SIGNETICS A-PACKAGE



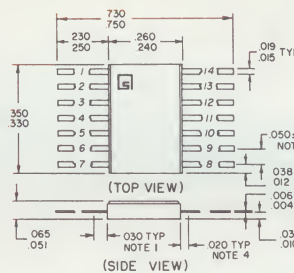
NOTES:

- (1) Lead spacing shall be measured within this zone.
- (2) Molded Plastic Body.
- (3) Kovar Leads.
- (4) Lead spacing tolerances are non-cumulative.
- (5) Thermal resistance from junction to still air, $\Theta_{JA} = 0.16^\circ\text{C}/\text{mW}$.
- (6) Leads shown as positioned by Signetics dual in-line package carrier.
- (7) All dimensions of plastic package exclude molding-caused flash.



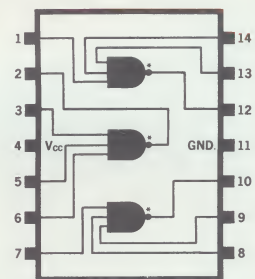
*No pull-up provided

S8471J N8471J J-PACKAGE (TO-88) (MODULAR GLASS-KOVAR)



NOTES:

- (1) Recommended minimum offset before lead bend.
- (2) All leads weldable and solderable.
- (3) All dimensions in inches.
- (4) Lead spacing dimensions apply to this area only.
- (5) Spacing tolerances non-cumulative.
- (6) Thermal resistance from junction to still air, $\Theta_{JA} = 0.3^\circ\text{C}/\text{mW}$.



*No pull-up provided

S8471A
S8471J
N8471A
N8471J



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AUGUST 1967

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 12,)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8471	TEMP. N8471	V _{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-4	"1" OUTPUT LEAKAGE CURRENT			25	μA	+125°C	+75°C	5.0V	0.6V			11
A-5	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	8.2mA	8
A-3				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	8.2mA	8
A-4				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	8.2mA	8
C-1	"0" INPUT CURRENT	-0.1		-0.8	mA	-55°C	0°C	5.25V	0.35V	5.25V		
A-3		-0.1		-0.8	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-0.8	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	PAIR DELAY (Figure 1)	50		150	ns	+25°C	+25°C	5.0V			D.C. F.O. = 9	9
C-2	FALL TIME (Figure 2)			75	ns	-55°C	0°C	4.75V			A.C. F.O. = 2	10
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			15	mW	+25°C	+25°C	5.0V				
	(Per Gate) OUTPUT "1"			4.5	mW	+25°C	+25°C	5.0V	0V			
A-2	INPUT VOLTAGE RATING	6.0			V	+25°C	+25°C	5.0V	50μA	0V		
A-2	OUTPUT VOLTAGE RATING	6.0			V	+25°C	+25°C	5.0V	0V			13

NOTES

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. $f = 1\text{MHz}$, $V_{ac} = 25\text{mVrms}$. All pins not specifically referenced are tied to guard for capacitance tests.
8. Output sink current is supplied through a resistor to V_{cc} .
9. One DC fan-out is defined as 0.8mA.
10. One AC fan-out for the 8400 Gates is defined as the clock input of an 8424 or 50pf.
11. Connect an external 1K ± 1 percent resistor from V_{cc} to the output terminal for this test.
12. Manufacturer reserves the right to make design and process changes and improvements.
13. Connect an external 1K ± 1 percent resistor from 6.3V to the output terminal.

FIGURE 1 — PAIR DELAY

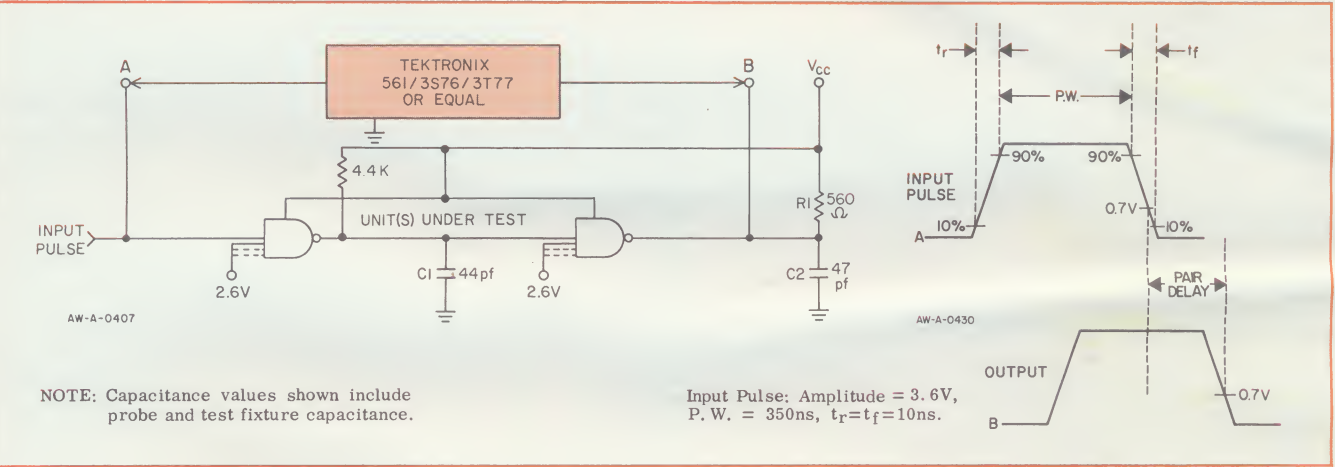
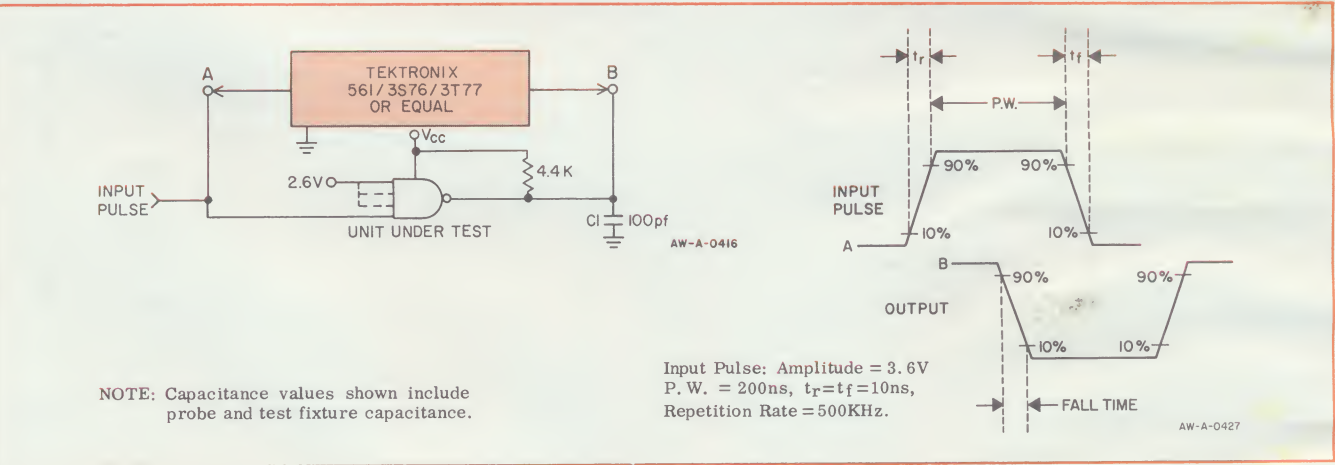


FIGURE 2 — FALL TIME



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LOW POWER
MONOLITHIC DCL ELEMENTS8471A
S8471J
N8471A
N8471J

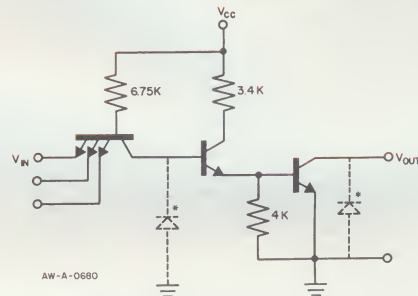
AUGUST 1967

S8471A, S8471J TRIPLE THREE-INPUT TTL NAND GATE (−55°C to +125°C)
N8471A, N8471J TRIPLE THREE-INPUT TTL NAND GATE (0°C to + 75°C)

The 8471 is a Triple, 3-Input NAND Gate with bare output collectors. Absence of any output pull-up structure allows the user complete freedom in the use of the 8471 in collector-logic (wired-AND) and similar applications. Proper pull-up resistor selection will allow as many as 30 outputs to be tied together. Attention must be given to the "1" DC noise margin and the "0" fan-out when selecting a pull-up resistor.

These devices are additional elements to the S8000J product line. For electrical characteristic curves, refer to the S8480J electrical characteristic curves in the S8000J data handbook.

BASIC CIRCUIT SCHEMATIC



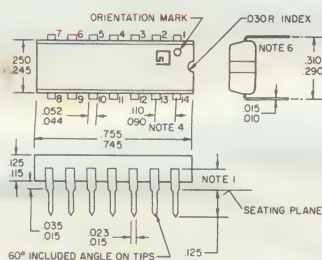
NOTE: 1/2 of unit shown. Component values are typical.
* Isolation diodes

ABSOLUTE MAXIMUM RATINGS

INPUT VOLTAGE	+6.0V
OUTPUT VOLTAGE	+6.0V
V _{cc}	+6.0V
INPUT CURRENT	±10mA

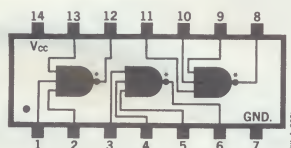
Maximum ratings are limiting values above which serviceability may be impaired.

OUTPUT CURRENT	+30, -10mA
OPERATING TEMPERATURE (S8471) (N8471)	−55°C to +125°C 0°C to +75°C
STORAGE TEMPERATURE	−65°C to +150°C
JUNCTION TEMPERATURE	+150°C

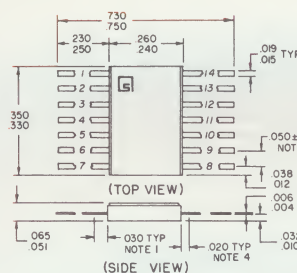
S8471A
N8471A
SIGNETICS A-PACKAGE

NOTES:

- (1) Lead spacing shall be measured within this zone.
- (2) Molded Plastic Body.
- (3) Kovar Leads.
- (4) Lead spacing tolerances are non-cumulative.
- (5) Thermal resistance from junction to still air, $\Theta_{JA} = 0.16^\circ\text{C}/\text{mW}$.
- (6) Leads shown as positioned by Signetics dual in-line package carrier.
- (7) All dimensions of plastic package exclude molding-caused flash.

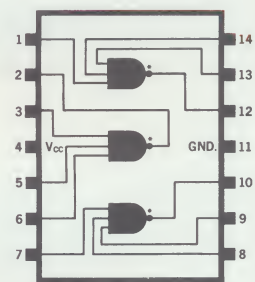


*No pull-up provided

S8471J
N8471J
J-PACKAGE (TO-88)
(MODULAR GLASS-KOVAR)

NOTES:

- (1) Recommended minimum offset before lead bend.
- (2) All leads weldable and solderable.
- (3) All dimensions in inches.
- (4) Lead spacing dimensions apply to this area only.
- (5) Spacing tolerances non-cumulative.
- (6) Thermal resistance from junction to still air, $\Theta_{JA} = 0.3^\circ\text{C}/\text{mW}$.



*No pull-up provided

S8471A
S8471J
N8471A
N8471J

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 12,)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8471	TEMP. N8471	V _{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-4	"1" OUTPUT LEAKAGE CURRENT			25	μA	+125°C	+75°C	5.0V	0.6V			11
A-5	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	8.2mA	8
A-3				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	8.2mA	8
A-4				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	8.2mA	8
C-1	"0" INPUT CURRENT	-0.1		-0.8	mA	-55°C	0°C	5.25V	0.35V	5.25V		
A-3		-0.1		-0.8	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-0.8	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	PAIR DELAY (Figure 1)	50		150	ns	+25°C	+25°C	5.0V			D.C. F.O. = 9	9
C-2	FALL TIME (Figure 2)			75	ns	-55°C	0°C	4.75V			A.C. F.O. = 2	10
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			15	mW	+25°C	+25°C	5.0V				
	(Per Gate) OUTPUT "1"			4.5	mW	+25°C	+25°C	5.0V	0V			
A-2	INPUT VOLTAGE RATING	6.0			V	+25°C	+25°C	5.0V	50μA	0V		
A-2	OUTPUT VOLTAGE RATING	6.0			V	+25°C	+25°C	5.0V	0V			13

NOTES

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance

8. tance Bridge or equivalent. $f = 1\text{MHz}$, $V_{ac} = 25\text{mVrms}$. All pins not specifically referenced are tied to guard for capacitance tests.
9. Output sink current is supplied through a resistor to V_{cc} .
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out for the 8400 Gates is defined as the clock input of an 8424 or 50pf.
12. Connect an external 1K ± 1 percent resistor from V_{cc} to the output terminal for this test.
13. Manufacturer reserves the right to make design and process changes and improvements.
14. Connect an external 1K ± 1 percent resistor from 6.3V to the output terminal.

FIGURE 1 — PAIR DELAY

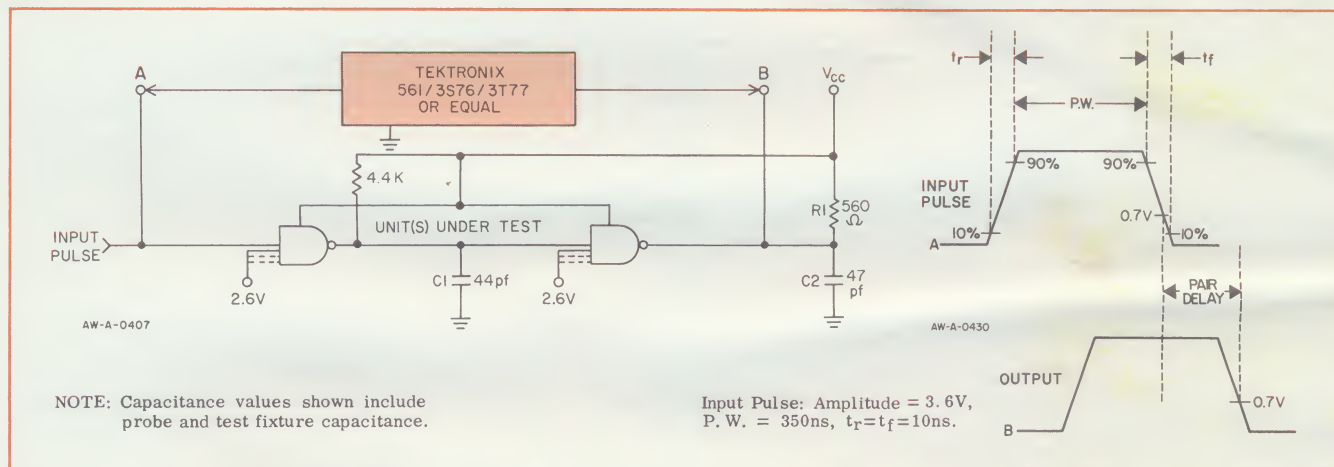
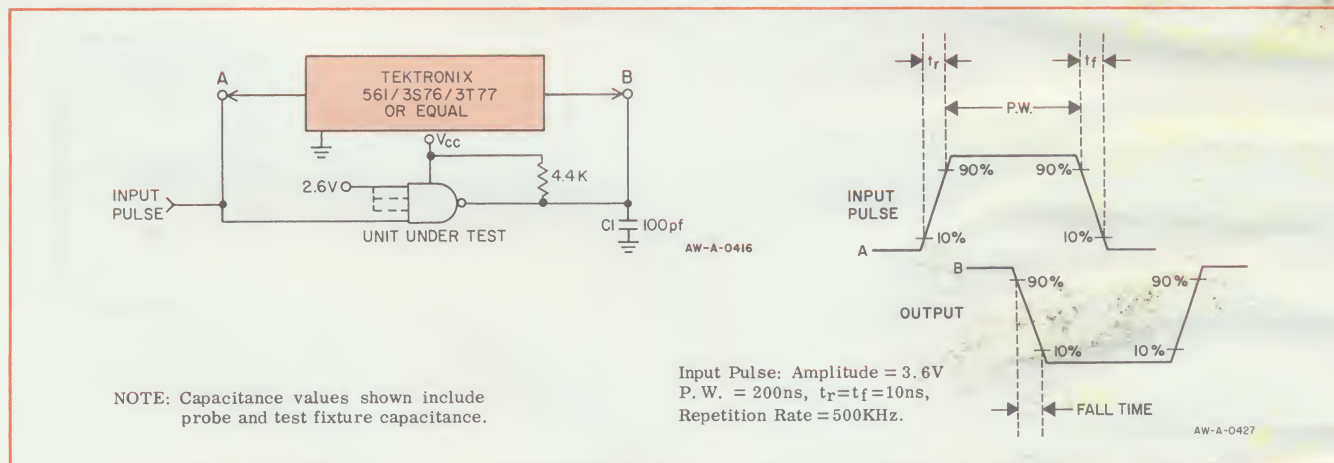


FIGURE 2 — FALL TIME



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PRELIMINARY SPECIFICATIONS

**LOW POWER
MONOLITHIC DCL ELEMENT**



**S8481A
S8481J
N8481A
N8481J**

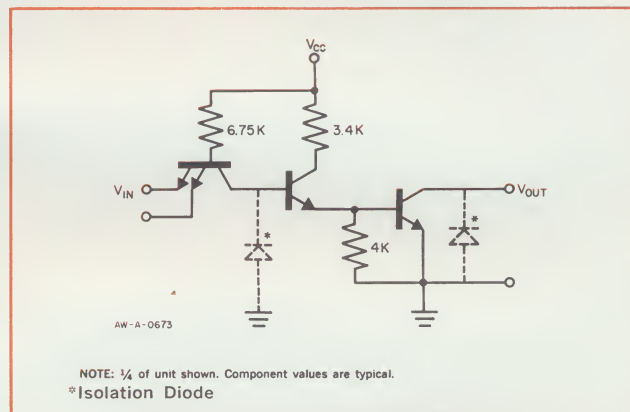
JULY 1967

S8481A, S8481J QUADRUPLER TWO-INPUT TTL NAND GATE (−55°C to +125°C)
N8481A, N8481J QUADRUPLER TWO-INPUT TTL NAND GATE (0°C to +75°C)

The 8481 is a Quadruple, 2-Input NAND Gate with bare output collectors. Absence of any output pull-up structure allows the user complete freedom in the use of the 8481 in collector-logic (wired-AND) and similar applications. Proper pull-up resistor selection will allow as many as 30 outputs to be tied together. Attention must be given to the "1" DC noise margin and the "0" fan-out when selecting a pull-up resistor.

These devices are additional elements to the S8000J product line. For electrical characteristic curves, refer to the S8480J electrical characteristic curves in the S8000J data handbook.

BASIC CIRCUIT SCHEMATIC

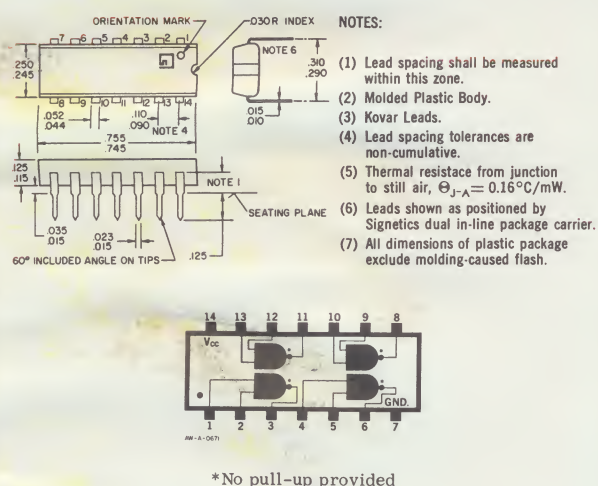


ABSOLUTE MAXIMUM RATINGS

INPUT VOLTAGE	+6.0V	OUTPUT CURRENT	+30, -10mA
OUTPUT VOLTAGE	+6.0V	OPERATING TEMPERATURE (S8481)	−55°C to +125°C
V _{cc}	+6.0V	(N8481)	0°C to +75°C
INPUT CURRENT	±10mA	STORAGE TEMPERATURE	−65°C to +150°C
		JUNCTION TEMPERATURE	+150°C

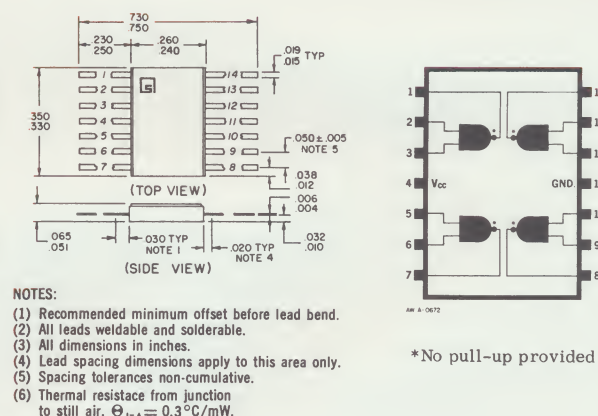
Maximum ratings are limiting values above which serviceability may be impaired.

**S8481A
N8481A
SIGNETICS A-PACKAGE**



*No pull-up provided

**S8481J
N8481J
J-PACKAGE (TO-88)
(MODULAR GLASS-KOVAR)**



*No pull-up provided



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**S8481A
S8481J
N8481A
N8481J**

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 12,)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8481	TEMP. N8481	V _{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-4	"1" OUTPUT LEAKAGE CURRENT			25	μA	+125°C	+75°C	5.0V	0.6V			11
A-5	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	8.2mA	8
A-3				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	8.2mA	8
A-4				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	8.2mA	8
C-1	"0" INPUT CURRENT	-0.1		-0.8	mA	-55°C	0°C	5.25V	0.35V	5.25V		
A-3		-0.1		-0.8	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-0.8	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	PAIR DELAY (Figure 1)	50		150	ns	+25°C	+25°C	5.0V			D.C. F.O. = 9	9
C-2	FALL TIME (Figure 2)			75	ns	-55°C	0°C	4.75V			A.C. F.O. = 2	10
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0" (Per Gate)			15	mW	+25°C	+25°C	5.0V				
A-2	OUTPUT "1"			4.5	mW	+25°C	+25°C	5.0V	0V			
A-2	INPUT VOLTAGE RATING	6.0			V	+25°C	+25°C	5.0V	50μA	0V		

NOTES

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. $f = 1 \text{ MHz}$, $V_{AC} = 25 \text{ mV}_{RMS}$. All pins not specifically referenced are tied to guard for capacitance tests.

8. Output sink current is supplied through a resistor to V_{CC} .
9. One DC fan-out is defined as 0.8mA.
10. One AC fan-out for the 8400 Gates is defined as the clock input of an 8424 or 50pf.
11. Connect an external 1K resistor from V_{CC} to the output terminal for this test.
12. Manufacturer reserves the right to make design and process changes and improvements.

FIGURE 1 — PAIR DELAY

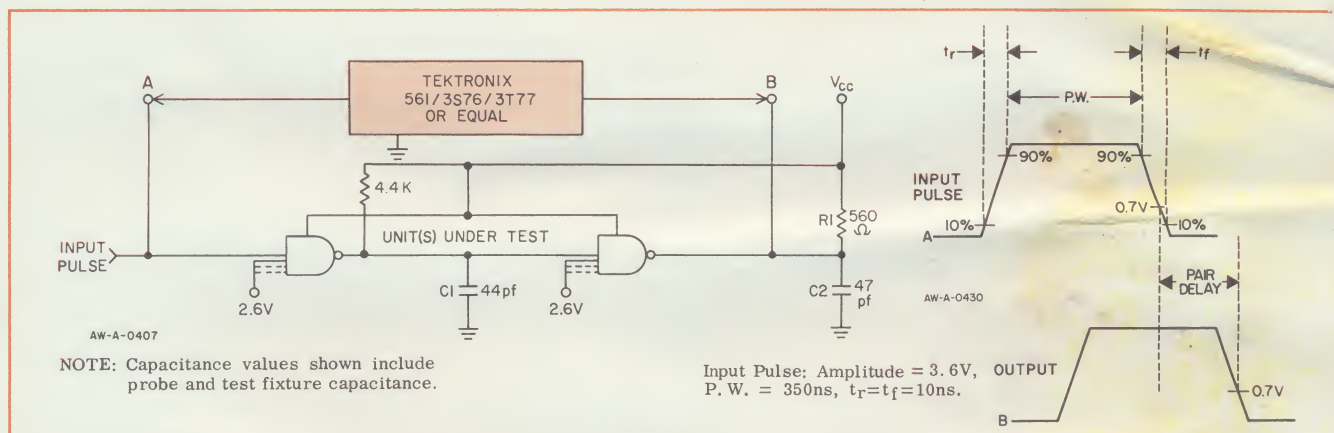
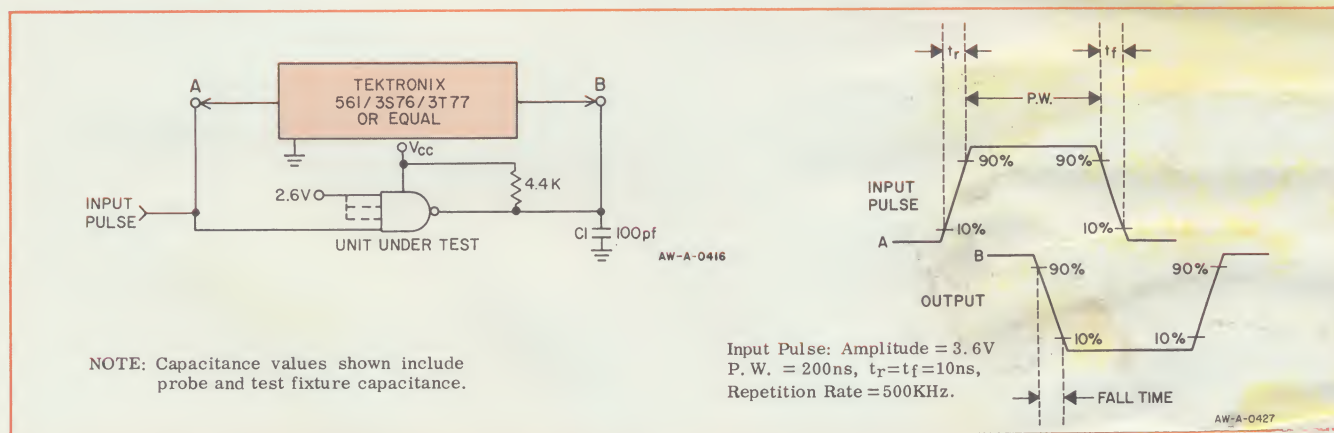


FIGURE 2 — FALL TIME



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